

As recited in amended claims 1 and 6, a novel features of the present invention resides in a semiconductor device comprising through holes, which are provided in a region between two semiconductor components, and which substantially eliminate the electrical interference between the two semiconductor components. According to the claimed invention, when high frequency signals are applied to one of the semiconductor components, leakage of the high frequency signals to another semiconductor component can be suppressed. Thus, the effect of maintaining isolation between the two semiconductor components can be achieved.

On the other hand, Fujita relates to a semiconductor device for holding wiring conductors having many through hole conductors in a high density three-dimensional lamination. Fujita teaches a plurality of through holes 5 formed in a semiconductor substrate 1, and the through holes are inserted with conductive pins 6 which are connected electrically by leads 7 to wiring conductors 3 connected to a large number of active devices 2. As such, the structure disclosed in Fujita is used for disposing a multiple pins semiconductor device on the semiconductor substrate.

Applicants respectfully submit that the semiconductor device of Fujita achieves a completely different purpose and does not teach the effect of maintaining isolation between two semiconductor components. Hence, Fujita clearly does not teach every features of the claimed invention as recited in amended claims 1 and 6.

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick, 221 USPQ 481, 485 (Fed. Cir. 1984). Fujita clearly fails to disclose every features positively recited and claimed in Applicants' independent claims 1 and 6, as well as their respective dependent claims.

With respect to the §103(a) rejection, the arguments set forth above in relation to the §102(b) are also applicable to the §103(a) rejection of claims 2, 5, and 7. Further, as Fujita does not teach the claimed features including the effect of maintaining isolation between two semiconductor components, there is no motivation to modify Fujita to provide a gap to be smaller than the thickness of the substrate, as recited in claim 2.

Having responded to all rejections set forth in the outstanding non-final Office Action, it is submitted that the claims are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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MARKED-UP COPY OF AMENDED CLAIMS

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;
at least two semiconductor components provided on the principal surface of the substrate; and
multiple through holes, which pass from the principal surface through the backside of the substrate and are provided in a region of the substrate between the at least two components so as to substantially eliminate the electrical interference between the two semiconductor components.

6. (Amended) A semiconductor device comprising:

a semiconductor substrate;
at least two semiconductor components provided on the principal surface of the substrate;
electrodes of the at least two components provided on the substrate so as to substantially eliminate the electrical interference between the two semiconductor components;
a first group of through holes, which pass from the principal surface through the backside of the substrate and are provided in respective regions of the substrate under the electrodes;
a first conductor film provided on the side faces of the first group of through holes;
a second group of through holes, which pass from the principal surface through the backside of the substrate and are provided in a region of the substrate between the components;
a second conductor film provided on the side faces of the second group of through holes; and
a wiring layer, which is provided on the backside of the substrate and is in contact with the first and second conductor films.